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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,452	09/05/2003	Mark Ellsberry	44223-0100	8437

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,452	ELLSBERRY ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 6, 8, 9, 11, 12, 15 - 24 and 27 - 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 - 6, 8, 9, 11 and 12* is/are allowed.

6)☒ Claim(s) *15, 17 - 20, 23, 24 and 28 - 32* is/are rejected.

7)☒ Claim(s) *16,21,22 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 15, 2005 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on February 15, 2005 has been received and entered in the case.

Claim Objections

3. Claim 20 is objected to because of the following informalities: in line 5, "plurality chip-scale" should be -- plurality of chip-scale --. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 28 – 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. In claim 28, line 3, "the memory die" lacks antecedent basis.

b. In claims 29 and 30, line 3, the term "substantially" is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 15, 17 – 19, 28, 29, 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Kyougoku et al. (U. S. Pat. No. 5,995,379).

Regarding claim 15, Kyougoku et al. discloses in e.g., Fig. 8 and Fig. 9 a stackable electronic assembly comprising:

- a plurality of chip-scale package, the plurality of chip-scale packages arranged in a stacked configuration, each chip-scale package including
    - o a substrate (70; column 8, line 67) having a first surface and an opposite second surface; the substrate composed of a controlled thermal expansion

material (column 5, lines 11 – 12; any ceramics or glass material inherently has some level or degree of controlled thermal expansion character. Thus, Kyougoku et al. discloses the limitation, "a controlled thermal expansion material");

- a semiconductor device (3; column 8, line 67) coupled to traces on the first surface of the substrate using underside coupling members (terminals under the chip 3; column 5, lines 45 – 46);
- a plurality of solder balls (5; column 5, lines 12 – 13) mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device (see e.g., Fig. 8), at least one of the solder balls electrically coupled to the semiconductor device (by the conductive traces between the element 5 and the chip 3, see e.g., Fig. 8); and
- a plurality of pads (11' and 12'; see e.g., Fig. 9) coupled to the second surface of the substrate (70), each pad electrically coupled to one or more of the plurality of solder balls (5 and 6) in a staggered routing scheme (see e.g., Fig. 9),
- wherein all chip-scale packages in the stacked configuration have identical routing traces (column 3, lines 34 – 35 and column 9, lines 54 – 55).

Regarding claim 17, Kyougoku et al. discloses in e.g., Fig. 8 and Fig. 9 the solder balls (5) on the first surface of a first chip-scale package being coupled to the pads (41 and 42) on the second surface of a second chip-scale package (see e.g., Fig. 9).

Regarding claim 18, Kyougoku et al. discloses in e.g., Fig. 8 and Fig. 9 the staggered routing scheme causing a solder ball (5) of a first chip-scale package of a stack configuration to be uniquely electrically coupled with an underside coupling member of a semiconductor device (4) mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two (column 9, lines 61 – 62 and Fig. 5).

Regarding claim 19, Kyougoku et al. discloses in e.g., Fig. 5 the staggered routing scheme being stepped as it moves up the plurality of chip-scaled packages of a stacked configuration (see Fig. 5).

Regarding claim 28, Kyougoku et al. discloses in e.g., Fig. 8 and Fig. 9 the semiconductor device (3) having a first surface and an opposite second surface, the first surface of the semiconductor device (3) mounted towards the first surface of the substrate (70), wherein the second surface of the memory die (3; column 5, lines 6 – 9) remains completely exposed for improved ventilation (see e.g., Fig. 8).

Regarding claim 29, Kyougoku et al. discloses in e.g., Fig. 8 and Fig. 9 five sides of the semiconductor device (3) being completely exposed and the first surface of the memory device (3) being "substantially" exposed for improved heat dissipation.

Regarding claim 31, Kyougoku et al. discloses in e.g., Fig. 6, Fig. 8 and Fig. 9 the staggered routing scheme forming an electrical path from a first chip-scale package of a stacked configuration that moves inward toward the semiconductor device (4) mounted on a second chip-scale package N levels from the first chip-scale package (see e.g., Figs. 8 and 9), where N is an integer greater than two (column 9, lines 61 – 62 and Fig. 5), as the electrical path moves up through each layer of the stacked configuration (see e.g., Figs. 5, 8 and 9).

Regarding claim 32, Kyougoku et al. discloses in e.g., Fig. 8 and Fig. 9 the electrical path moving from the first chip-scale package of a stacked configuration to a last chip-scale package of the stacked configuration along one side of the stacked configuration (see e.g., Figs. 5, 8 and 9).

8. Claims 20 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Moden et al. (U. S. Pat. No. 6,297,960).

Regarding claim 20, Moden et al. disclose in e.g., Fig. 4 a memory module comprising:

- a main substrate (12; column 3, line 14) with an interface to couple the memory module to other devices (see e.g., Fig. 4); and
- one or more stacks of memory devices (100, at the top of the main substrate 12; column 1, lines 16 – 25 and column 3, lines 22 – 23) coupled to a first surface of the main substrate,
    - at least one stack of memory devices including
    - a plurality of chip-scale packages, the plurality of chip-scale packages arranged in a stack, all chip-scale packages in the stack having identical routing traces at every level of the stack (see e.g., Fig. 4), each chip-scale package (column 3, lines 21 – 30) including
        - a substrate (104; column 3, line 24) having a first surface and an opposite second surface,

- a memory semiconductor die (DIE or 102; column 3, lines 23 – 24 and column 1, lines 16 – 25) electrically coupled to traces on the first surface of the substrate, and
- a plurality of solder balls (106; column 3, line 34) mounted on the first surface of the substrate adjacent to the memory semiconductor die (see e.g., Fig. 4), at least one of the solder balls electrically coupled to the memory semiconductor die (column 5, lines 33 – 39).

Regarding claim 24, Moden et al. disclose in e.g., Fig. 4 one or more stacks of memory devices (100, at the bottom; column 3, lines 22 – 23) coupled to a second surface of the main substrate.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moden et al. in view of Yew et al. (U. S. Pat. No. 6,137,164).

While Moden et al. discloses the memory module (100), Moden et al. does not disclose the memory module being a dual inline memory module. Yew et al. teaches in e.g., Fig. 4A a memory module (420) being a dual inline memory module (DIMM; column 5, lines 7 – 23). It would have been obvious to one of ordinary skill in the art at the time when the invention was

made to apply the dual inline memory module of Yew et al. into the structure of Moden et al. as taught by Yew et al. to have printed interconnect circuitry on both surface by improving packing density and performance of integrated circuits devices (column 5, lines 17 – 18 and column 3, lines 18 – 19).

11. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kyougoku et al. in view of Nishimura et al. (U. S. Pat. No. 6,781,241).

While Kyougoku et al. discloses the semiconductor device (3) mounted on the first surface of the substrate (70), Kyougoku et al. does not disclose one or more electrical components mounted on the second surface of the substrate. Nishimura et al. teaches in e.g., Fig. 4 one or more electrical components (3a; column 5, lines 13 – 14) mounted on the second surface of a substrate (1a; column 5, line 13) in an area "substantially" opposite of a semiconductor device (3c or 3b; column 7, line 8), wherein the combined distance that an electronic component (3a) and the semiconductor device (3b) protrude from the substrate (1a) is less than the distance that a solder ball (7; column 5, line 20) and pad (5a; see Fig. 2 and column 5, line 63) protrude from the substrate (column 5, line 66 – column 6, line 1). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the electrical components of Nishimura et al. onto the second surface of the substrate of Kyougoku et al. as taught by Nishimura et al. to reduce thickness of the semiconductor device (column 6, lines 16 – 19).

Allowable Subject Matter

12. Claims 1 – 6, 8, 9, 11 and 12 are allowed.

a. The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or reasonably suggest, either singularly or in combination, at least a substrate having a coefficient of expansion that matches a coefficient of expansion of a memory die to within six parts per million per degree Celsius or less, wherein the second surface of the memory die remains completely exposed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

13. Claims 16, 21, 22 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

a. Claims 16, 21 and 27 contain allowable subject matter because none of references of record teach or suggest, either singularly or in combination, at least the limitation of a substrate having a coefficient of expansion that matches a coefficient of expansion of a memory die to within six parts per million per degree Celsius or less, wherein the second surface of the memory die remains completely exposed.

b. Claim 22 is a dependent claim of objected claim (claim 21), this claim is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (e.g., claim 21).

Response to Arguments

14. Applicant's arguments with respect to claim 15 and 20 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Wednesday, April 06, 2005

GEORGE ECKERT
PRIMARY EXAMINER